CLAIMS

What is claimed is:

1. An integrated circuit, comprising:

a substrate comprising:

core logic circuitry;

isolation cell circuitry; and

an embedded memory coupled to the core logic circuitry,

wherein the embedded memory is capable of being electrically isolated from the core logic circuitry by the isolation cell circuitry.

2. The integrated circuit of Claim 1, wherein the embedded memory has input and output.

3. The integrated circuit of Claim 2, wherein the isolation cell circuitry includes a first isolation cell and a second isolation cell.

4. The integrated circuit of Claim 3, wherein the input of the embedded memory is isolated from the core logic circuitry by the first isolation cell and the output of the embedded memory is isolated from the core logic circuitry by the second isolation cell.

5. The integrated circuit of Claim 4, wherein the input of the embedded memory is controlled by a power level of the core logic circuitry.

6. The integrated circuit of Claim 5, further comprising input/output circuitry coupled to the core logic circuitry for transferring data to and from the integrated circuit.

7. The integrated circuit of Claim 6, wherein the input of the embedded memory is controlled by a power level of the input/output circuitry.

8. The integrated circuit of Claim 7, further comprising analog circuitry coupled to the core logic circuitry.

9. The integrated circuit of Claim 8, wherein the input of the embedded memory is controlled by a power level of the analog circuitry.

10. The integrated circuit of Claim 9, wherein the input of the embedded memory is controlled by the power levels of the core logic circuitry, the input/output circuitry, and the analog circuitry through a totem pole arrangement of transistors.

11. The integrated circuit of Claim 10, wherein the input of the embedded memory is applied to gate terminals of two transistors included in the totem pole arrangement of transistors.

12. An isolation cell for isolating an embedded memory from other circuitry on an integrated circuit, comprising:

a totem pole arrangement of switches such that each drain and source terminal the switches are connected to one of the group consisting of drain terminals of other switches in the totem pole arrangement, source terminals of other switches in the totem pole arrangement, power, and ground, the totem pole arrangement of switches receiving signal for an embedded memory, the totem pole arrangement of switches providing an output signal to the embedded memory; and

a latch circuit for latching the output signal from the totem pole arrangement of switches, the output signal being supplied to the embedded memory.

13. The isolation cell of Claim 12, the totem pole arrangement of switches including a switch controlled by a power level of core logic circuitry on the integrated circuit.

14. The isolation cell of Claim 13, the totem pole arrangement of switches further including a switch controlled by a power level of input and output circuitry on the integrated circuit.

15. The isolation cell of Claim 14, the totem pole arrangement of switches further including a switch controlled by a power level of analog circuitry on the integrated circuit.

16. The isolation cell of Claim 15, the totem pole arrangement of switches further comprising a switch controlled by a first enable signal and a switch controlled by a second enable signal.

17. The isolation cell of Claim 16, wherein the first and second enable signals are electrically connected to ground through pull down resistors.

18. A method for isolating an embedded memory on an integrated circuit, comprising:

Detecting a power level drop below a power threshold level for non-storage circuitry on an integrated circuit; and

Disabling input to and output from an embedded memory on the integrated circuit in response to the power level drop of the core logic circuitry.

19. The method of Claim 18, wherein the non-storage circuitry is core logic circuitry.

20. The method of Claim 18, wherein the non-storage circuitry is analog circuitry.

21. The method of Claim 18, wherein the non-storage circuitry is input/output interface circuitry.

22. The method of Claim 18, wherein the embedded memory is electrically isolated from core logic, input and output, and analog circuitry through at least one isolation cell.

23. The method of Claim 1, further comprising, if power is being applied to the core, input and output, and analog circuitry, enabling data transfer to and from the embedded memory by at least one enable signal.

24. An integrated circuit, comprising:

an embedded memory; and

isolation circuitry for preventing data transfers to and from the embedded memory when a power level on the integrated circuit falls below a predetermined threshold.

25. The isolated embedded memory of Claim 24, wherein the power level is a power level of core logic circuitry on the integrated circuit.

26. The isolated embedded memory of Claim 24, wherein the power level is a power level of input and output circuitry on the integrated circuit.

27. The isolated embedded memory of Claim 24, wherein the power level is a power level of analog circuitry on the integrated circuit.

28. The isolated embedded memory of Claim 24, wherein the integrated circuit is a redundant array of independent disks (RAID) input/output controller chip.

29. An integrated circuit having an embedded memory, comprising:

embedded means for storing data located on a substrate;

means for isolating the embedded means for storing data, the isolating means capable of preventing data to be written to the embedded means for storing data when a power fault is detected on the integrated circuit.

30. The integrated circuit of Claim 29, further comprising means for providing core logic, the means for providing core logic being coupled to the embedded means for storing data through the isolating means.

31. The integrated circuit of Claim 30, further comprising means for inputting signals from an external device to the integrated circuit and for output signals from the integrated circuit to the external device.

32. The integrated circuit of Claim 31, wherein the means for inputting and outputting is coupled to the means for providing core logic.

33. The integrated circuit of Claim 32, wherein the embedded means for storing data and the isolating means share a power supply.

34. The integrated circuit of Claim 33, wherein the power supply for the embedded means for storing data and the isolating means is dedicated such that the embedded means for storing data and the isolating means are the only circuitry that uses that power supply on the integrated circuit.

35. The integrated circuit of Claim 34, wherein the power supply aforementioned is a first power supply, the means for providing core logic using a second power supply and the means for inputting and outputting using a third power supply.

36. The integrated circuit of Claim 35, further comprising means for performing analog circuit operations, the means for performing analog circuit operations coupled to the means for providing core logic.

37. The integrated circuit of Claim 36, wherein the means for performing analog circuit operations includes analog circuitry.

38. The integrated circuit of Claim 37, wherein the means for performing analog circuit operations uses a fourth power supply, wherein the first, second, third, and fourth power supplies are distinct.